IN THE CLAIMS:

1. (Withdrawn) A method of manufacturing an active matrix pixel device comprising a thin film transistor (10) which includes a polycrystalline silicon channel (15) and doped source/drain regions (16,17), and a PIN diode (12) which includes a p-type doped region (26) and an n-type doped region (24) separated by an amorphous silicon intrinsic region (25), the method including the steps of: (a)--forming a plurality of polycrystalline silicon islands on a substrate (14), one of which providing the transistor channel (15), and source/drain regions (16,17); and then, (b)--depositing and patterning a layer of amorphous silicon to provide the intrinsic region (25) of the PIN diode (12) such that the intrinsic region overlies and contacts at least a part of one of the polycrystalline silicon islands which provides one of the p-type or n-type doped regions.

2. (Withdrawn) A method according to claim 1, wherein the source/drain regions (16,17) and said one of the p-type or n-type doped regions (26,24) of the PIN diode are provided by the same polycrystalline silicon island.

3. (Withdrawn) A method according to claim 1, wherein the source/drain regions are doped n-type, and wherein the method further comprises the steps of: (c)--depositing and patterning a layer of aluminum to define a top PIN diode contact (40) on the intrinsic region (25) of the PIN diode; (d)--annealing the top PIN diode contact to cause aluminum ions to diffuse into the underlying intrinsic region to form the p-type doped region (26).

4. (Withdrawn) A method according to claim 3, further comprising the step of: (e)--etching away part of the top PIN diode contact (40) so as to expose the PIN diode to input light (100).

5. (Currently amended) An active matrix pixel device comprising a plurality of polycrystalline silicon islands supported by a substrate ~~(14)~~, one of the polycrystalline silicon islands providing a channel ~~(15)~~ and doped source/drain regions ~~(16,17)~~ of a thin

film transistor ~~(10)~~, the active matrix pixel device further comprising a PIN diode ~~(12)~~ which includes a p-type doped region ~~(26)~~ and an n-type doped region ~~(24)~~ separated by an amorphous silicon intrinsic region ~~(25)~~, wherein the amorphous silicon intrinsic region overlies and contacts at least a part of one of the polycrystalline silicon islands which provides one of the p-type or n-type doped regions of the PIN diode.

6. (Currently amended) An active matrix pixel device according to claim 5, wherein the doped source/drain regions ~~(16,17)~~ and said one of the p-type or n-type doped regions ~~(26,24)~~ of the PIN diode are provided by the same polycrystalline silicon island.

7. (Original) An active matrix pixel device according to claim 5, wherein both the p-type and n-type doped regions of the PIN diode are provided by respective ones of the polycrystalline silicon islands.

8. (Currently amended) An active matrix pixel device according to claim 7, further comprising a second thin film transistor ~~(10b)~~ having doped source/drain regions ~~(16b,17b)~~ provided by one of the polycrystalline silicon islands, the doped source/drain regions ~~(16b,17b)~~ being of an opposite conductivity type to those of ~~the~~ a first thin film transistor ~~(16a,17a)~~, wherein the n-type doped region ~~(24)~~ of the PIN diode is provided by a doped source/drain region ~~(17a)~~ of one transistor and the p-type doped region ~~(26)~~ of the PIN diode is provided by a doped source/drain region ~~(16b)~~ of the other transistor.

9. (Currently amended) An active matrix pixel device according to claim 7, wherein a transparent conductive gate ~~(30)~~ overlies the amorphous silicon intrinsic region ~~(25)~~ of the PIN diode separated therefrom by an insulating layer ~~(18)~~, the gate serving to apply a voltage to the intrinsic region so as to control the conductivity between the n-type and p-type doped regions.

10. (Currently amended) An active matrix pixel device according to claim 5, wherein the thin film transistor further comprises a gate electrode ~~(20)~~ which serves to control ~~the~~ a current through the channel, and wherein the amorphous silicon intrinsic region of the

PIN diode overlies the gate electrode.

11. (Currently amended) An active matrix electroluminescent display device according to ~~claim 1~~ claim 5, wherein the PIN diode serves to measure ~~the~~ a light intensity output ~~(100)~~ from an associated display element and supply a signal to drive circuitry connected thereto to enable modulation of the light intensity output in accordance with the measured light intensity output.